IN THE CLAIMS:

Please add new claims 15-64 as follows:

- -15. (New) A method of switching between a predetermined plurality of instruction sets used by a data processing apparatus, the method comprising:

in response to a first instruction:

(i) accessing a sequence of bits, the sequence of bits having an address portion and an instruction set indicator portion;

(ii) identifying an instruction set selected from the predetermined plurality of instruction sets based on the instruction set indicator portion of the sequence of bits;

(iii) setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits; and

retrieving a second instruction from an address derived from the address portion of the sequence of bits,

wherein the instruction set identified by the instruction set indicator portion of the sequence of bits is identifiable without regard to the address derived from the address portion of the sequence of bits.

16. (New) The method of claim 15, further comprising executing the second instruction as an instruction of the current instruction set.

17. (New) The method of claim 15 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

18. (New) The method of claim 17 wherein X is 32 and Y is 16.

19. (New) The method of claim 15 wherein the instruction set indicator portion of the sequence of bits comprises one or more least significant bits of the sequence of bits.

20. (New) The method of claim 15 wherein the instruction set indicator portion of the sequence of bits comprises one or more most significant bits of the sequence of bits.

21. (New) A method of switching between a predetermined plurality of instruction sets used by a data processing apparatus, the method comprising:

in response to a first instruction:

(i) accessing a sequence of bits, the sequence of bits having an address portion and an instruction set indicator portion, the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits;

(ii) identifying an instruction set selected from the predetermined plurality of instruction sets based on the instruction set indicator portion of the sequence of bits;

(iii) setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits; and

retrieving a second instruction from an address derived from the address portion of the sequence of bits.

22. (New) The method of claim 21, further comprising executing the second instruction as an instruction of the current instruction set.

23. (New) The method of claim 21 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein

instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

24. (New) The method of claim 23 wherein X is 32 and Y is 16.

25. (New) The method of claim 21 wherein the instruction set indicator portion of the sequence of bits comprises one or more least significant bits of the sequence of bits.

26. (New) The method of claim 21 wherein the instruction set indicator portion of the sequence of bits comprises one or more most significant bits of the sequence of bits.

27. (New) A data processing apparatus capable of operating using instructions from a predetermined plurality of instruction sets, the data processing apparatus comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits, the sequence of bits having an address portion and an instruction set indicator portion, the processor core deriving an address of a second instruction from the address portion of the sequence of bits and using the instruction set indicator portion of the sequence of bits to set one or more control flags; and

(ii) a controller responsive to the one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets, to cause the processor core to execute the second instruction as an instruction from the current instruction set,

wherein the one or more control flags are set without regard to the address derived from the address portion of the sequence of bits.

28. (New) The apparatus of claim 27 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

29. (New) The apparatus of claim 27, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

30. (New) The apparatus of claim 27, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

31. (New) The apparatus of claim 27 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

32. (New) The apparatus of claim 31 wherein X is 32 and Y is 16.

33. (New) A data processing apparatus capable of operating using instructions from a predetermined plurality of instruction sets, the data processing apparatus comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits to derive an address of a second instruction, the sequence of bits having an address portion and an instruction set indicator portion and the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits, the address of the second instruction being derived from the address portion of the sequence of bits;

(ii) the processor core using the instruction set indicator portion of the sequence of bits to set one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets; and

(iii) a controller responsive to the one or more control flags to cause the processor core to execute the second instruction as an instruction from the current instruction set.

34. (New) The apparatus of claim 33 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

35. (New) The apparatus of claim 33, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

36. (New) The apparatus of claim 33, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

37. (New) The apparatus of claim 33 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

38. (New) The apparatus of claim 37 wherein X is 32 and Y is 16.

39. (New) A data processing architecture capable of operating using instructions from a predetermined plurality of instruction sets, the data processing architecture comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits, the sequence of bits having an address portion and an instruction set indicator portion, the processor core deriving an address of a second instruction from the address portion of the sequence of bits and using the instruction set indicator portion of the sequence of bits to set one or more control flags; and

(ii) a controller responsive to the one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets, to cause the processor core to execute the second instruction as an instruction from the current instruction set,

wherein the one or more control flags are set without regard to the address derived from the address portion of the sequence of bits.

40. (New) The data processing architecture of claim 39 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

41. (New) The data processing architecture of claim 39, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

42. (New) The data processing architecture of claim 39, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

43. (New) The data processing architecture of claim 39 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

44. (New) The data processing architecture of claim 43 wherein X is 32 and Y is 16.

45. (New) A data processing architecture capable of operating using instructions from a predetermined plurality of instruction sets, the data processing architecture comprising:

(i) a processor core responsive to a first instruction to access a sequence of bits to derive an address of a second instruction, the sequence of bits having an address portion and an instruction set indicator portion and the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits, the address of the second instruction being derived from the address portion of the sequence of bits;

(ii) the processor core using the instruction set indicator portion of the sequence of bits to set one or more control flags, the state of the one or more control flags specifying a current instruction set selected from the predetermined plurality of instruction sets; and

(iii) a controller responsive to the one or more control flags to cause the processor core to execute the second instruction as an instruction from the current instruction set.

46. (New) The data processing architecture of claim 45 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

47. (New) The data processing architecture of claim 45, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

48. (New) The data processing architecture of claim 45, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

49. (New) The data processing architecture of claim 45 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

50. (New) The data processing architecture of claim 49 wherein X is 32 and Y is 16.

51. (New) A data processing apparatus capable of switching between a predetermined plurality of instruction sets, the data processing apparatus comprising:

(i) means for accessing a sequence of bits in response to a first instruction, the sequence of bits having an address portion and an instruction set indicator portion;

(ii) means for identifying an instruction set selected from the predetermined plurality of instruction sets based on the instruction set indicator portion of the sequence of bits in response to the first instruction;

(iii) means for setting one or more control flags to indicate that a current instruction set for the data processing apparatus is the instruction set identified based on the instruction set indicator portion of the sequence of bits in response to the first instruction; and

(iv) means for retrieving a second instruction from an address derived from the address portion of the sequence of bits in response to the first instruction,

wherein the instruction set identified by the instruction set portion of the sequence of bits is identifiable without regard to the address derived from the address portion of the sequence of bits.

52. (New) The data processing architecture of claim 51 wherein the one or more control flags comprise one or more predetermined bits in a program counter.

53. (New) The data processing architecture of claim 51, further comprising a memory system, wherein the memory system is not responsive to the one or more control flags.

54. (New) The data processing architecture of claim 51, further comprising a memory system wherein the one or more control flags are not provided to the memory system.

55. (New) The data processing architecture of claim 51 in which the predetermined plurality of instruction sets comprises a first instruction set and a second instruction set, and wherein instructions of the first instruction set are X-bit instructions and instructions of the second instruction set are Y-bit instructions, where Y is different from X.

56. (New) The apparatus of claim 55 wherein X is 32 and Y is 16.

57. (New) A method of operating a data processing apparatus, the method comprising:

(i) receiving a first instruction from a first instruction set selected from a predetermined plurality of instruction sets;

(ii) translating the first instruction to generate a first set of one or more control signals;

(iii) accessing a sequence of bits comprising an address portion and an instruction set indicator portion in response to the first set of one or more control signals, the instruction set indicator portion having at least one bit that is not part of the address portion of the sequence of bits;

(iv) setting one or more control flags based upon the value of the instruction set indicator portion of the sequence of bits to specify that a current instruction set is a second instruction set selected from a predetermined plurality of instruction sets;

(v) retrieving a second instruction using an address derived from the address portion of the sequence of bits; and

(vi) translating the second instruction as an instruction from the current instruction set to generate a second set of one or more control signals.

58. (New) The method of claim 57 wherein the predetermined plurality of instruction sets consists of two instruction sets.

59. (New) The method of claim 57 wherein the first instruction set consists of X-bit instructions and the second instruction set consists of Y-bit instructions, Y being different from X.

60. (New) The method of claim 58 wherein the first instruction set consists of X-bit instructions and the second instruction set consists of Y-bit instructions, Y being different from X.

61. (New) The method of claim 59 wherein X is 32 and Y is 16.

62. (New) The method of claim 60 wherein X is 32 and Y is 16.

63. (New) The method of claim 59 wherein X is 16 and Y is 32.

64. (New) The method of claim 60 wherein X is 16 and Y is 32. - -

STATUS OF CLAIMS

The '265 patent issued with 14 claims. Upon entry of this Amendment, original claims 1-14 remain unamended and new claims 15-64 will have been added. Thus, the total number of pending claims will therefore be 64.

SUPPORT FOR CLAIM AMENDMENTS

New claim 15 and the claims dependent thereon (claims 16 through 20) are directed to a method of switching between a predetermined plurality of instruction sets used by a data processing apparatus. Support for these claims is provided throughout the specification, including without limitation at column 2, line 1 – column 3, line 2; column 3, lines 42-46; column 6, lines 23-53; column 7, lines 48-67 and the figures referenced therein. Additional support for the dependent claims is also found throughout the specification, including without limitation at column 3, lines 19-41; column 4, lines 44-60; and column 5, line 1- column 6, line 4 and in the accompanying figures.

New claim 21 and the claims dependent thereon (claims 22 through 26) are directed to a method of switching between a predetermined plurality of instruction sets used by a data processing apparatus. Support for these claims is provided throughout the specification, including without limitation at column 2, line 1 – column 3, line 2; column 3, lines 42-46; column 6, lines 23-53; column 7, lines 48-67 and the figures referenced therein. Additional support for the dependent claims is also found throughout the specification, including without limitation at column 3, lines 19-41; column 4, lines 44-60; and column 5, line 1- column 6, line 4 and in the accompanying figures.

New claim 27 and the claims dependent thereon (claims 28 through 32) are directed to a data processing apparatus capable of operating using a predetermined plurality of instruction sets. Support for these claims is found throughout the specification, including without limitation at column 2, line 1 - column 3, line 2; column 3, lines 42-46; column 4, lines 6-60; column 5,

line 1 – column 6, line 4; column 6, lines 23-53; column 7, lines 48-67; and in the figures referenced therein. Additional support for the dependent claims is also found throughout the specification, including without limitation at column 3, lines 19-46; column 4, lines 44-60; column 5, lines 30-48; and in the accompanying figures.

New claim 33 and the claims dependent thereon (claims 34 through 38) are directed to a data processing apparatus capable of operating using a predetermined plurality of instruction sets. Support for these claims is found throughout the specification, including without limitation at column 2, line 1 - column 3, line 2; column 3, lines 42-46; column 4, lines 6-60; column 5, line 1 – column 6, line 4; column 6, lines 23-53; column 7, lines 48-67; and in the figures referenced therein. Additional support for the dependent claims is also found throughout the specification, including without limitation at column 3, lines 19-46; column 4, lines 44-60; column 5, lines 30-48; and in the accompanying figures.

New claim 39 and the claims dependent thereon (claims 40 through 44) are directed to a data processing architecture that is capable of operating using a predetermined plurality of instruction sets. Support for these claims is found throughout the specification, including without limitation at column 2, line 1 - column 3, line 2; column 3, lines 42-46; column 4, lines 6-60; column 5, line 1 – column 6, line 4; column 6, lines 23-53; column 7, lines 48-67; and in the figures referenced therein. Additional support for the dependent claims is also found throughout the specification, including without limitation at column 3, lines 19-46; column 4, lines 44-60; column 5, lines 30-48; and in the accompanying figures.

New claim 45 and the claims dependent thereon (claims 46 through 50) are directed to a data processing architecture that is capable of operating using a predetermined plurality of instruction sets. Support for these claims is found throughout the specification, including without limitation at column 2, line 1 - column 3, line 2; column 3, lines 42-46; column 4, lines 6-60; column 5, line 1 – column 6, line 4; column 6, lines 23-53; column 7, lines 48-67; and in the figures referenced therein. Additional support for the dependent claims is also found

throughout the specification, including without limitation at column 3, lines 19-46; column 4, lines 44-60; column 5, lines 30-48; and in the accompanying figures.

New claim 51 and the claims dependent thereon (claims 52-56) are directed to a data processing apparatus capable of switching between a predetermined plurality of instruction sets. Support for these claims is provided throughout the specification, including without limitation at column 2, line 1 – column 3, line 2; column 3, lines 42-46; column 3, line 63 – column 4, line 14; column 4, lines 39-53; column 5, line 1- column 6, line 4; column 6, lines 23-53; and column 7, lines 48-67. Additional support for the dependent claims is also found throughout the specification, including without limitation at column 3, lines 19-46; column 4, lines 44-60; and column 5, lines 30-48; and in the accompanying figures.

New claim 57 and the claims dependent thereon (claims 58-64) are directed to a method of operating a data processing apparatus. Support for these claims is provided throughout the specification, including without limitation at column 2, line 1 – column 3, line 2; column 3, lines 10-46; column 3, line 63 – column 4, line 14; column 4, lines 39-53; column 5, line 1- column 6, line 4; column 6, lines 23-53; and column 7, lines 48-67. Additional support for the dependent claims is also found throughout the specification, including without limitation at column 3, lines 19-46 and column 4, lines 44-60 and the accompanying figures.

OFFER TO SURRENDER OF ORIGINAL LETTERS PATENT

Applicant hereby offers to surrender the original Letters Patent to the U.S. Patent and Trademark Office upon allowance of the reissue application.

FOREIGN PRIORITY CLAIMS

Applicant hereby claims priority to UK Patent Application 9411670.4, filed June 10, 1994.

CONCLUSION

It is respectfully submitted that grant of this reissue application is appropriate. Applicant submits that claims 1-14 remain patentable for the reasons of record and that new claims 15-61 are in condition for allowance, which action is hereby requested.

Any additional fees which may be due in connection with this filing should be charged to Deposit Account No. 23-1703.

Dated: February 1, 2002

Respectfully submitted,

Scott T. Weingaertner
Reg. No. 37,756
Attorney for Applicant

Customer No. 007470
Direct Dial: (212) 819-8404